

# BLAINE C. READLER

2011

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INDEPENDENT DIGITAL DEVELOPMENT ENGINEER: thirty years experience developing complex data communications systems; from architecture to component level design.

## FPGA Development

For the last six years I have focused exclusively on FPGA development. Prior to that, the projects included a mix of FPGA and board design. All work since 1996 has been on a contract basis. Unless otherwise noted, each project included high level architecture development (diagramed with Visio), modular coding, testbench development, simulation at both modular and top-block level, synthesis/build, and bench testing. All simulation was done with ModelSim. All devices were Xilinx unless otherwise noted.

<b>year:</b> 1997	<b>client:</b> Alcatel Data Networks, VA	<b>device:</b> XC4010XL	<b>language:</b> verilog	<b>synthesis:</b> Synplicity
<b>project:</b> multi-bus/multi-processor controller for a carrier-class packet switch. Interfaces included RS232, X.25, and Frame Relay.				
<b>year:</b> 1999-01	<b>client:</b> Timeplex (div. of Milgo), MD/NJ	<b>device:</b> Altera EPF10K100	<b>language:</b> VHDL	<b>synthesis:</b> vendor sw
<b>project:</b> A modular-interfaces, customer-premises ATM packet mux/switch. Over a period of four years, I developed the entire product for the client. The example included here is the largest FPGA: a dual-channel AAL1(CBR) circuit-emulation SAR. FIFO-adaptive rate adaptation provided synchronized circuit timing delivery across the asynchronous packet-based network.				
<b>year:</b> 2000-01	<b>client:</b> Ensemble Communications, San Diego	<b>device:</b> XCV2600-E	<b>language:</b> verilog	<b>synthesis:</b> Synopsis
<b>project:</b> I developed a large board for this client's broadband wireless edge-access switch, but also included were two FPGA tasks: 1) an ATM interface w/ high-feature UTOPIA interface as part of a multi-engineer FPGA/ASIC; 2) proprietary time-stamp (SRTS-like) rate recovery (we developed a patent from this).				
<b>year:</b> 2000-02	<b>client:</b> Calix, Petaluma, CA	<b>devices:</b> XCV300, XC2V1000	<b>language:</b> verilog	<b>synthesis:</b> Synplicity
<b>project:</b> carrier-class SONET mux/switch: 1) DS3 map/demap interface. Including DS3 de-synchronization (FIFO adaptive and SRTS clock recovery); 2) UTOPIA cell mux/demux interface; 3) SONET OC12 M13 support: VT time/space switching (x336) & OH processing.				
<b>year:</b> 2001, 03	<b>client:</b> AirFiber, San Diego	<b>devices:</b> XC2S100, XC2V??	<b>language:</b> verilog	<b>synthesis:</b> vendor sw
<b>project:</b> two projects for this client's ATM switch: 1) cell throttling FPGA -- limiting the average cell bandwidth based on policing parameters; 2) I/Q coding, rate conversion, clocking support				
<b>year:</b> 2001	<b>client:</b> ViaSat, Carlsbad, CA	<b>device:</b> XCV2000-E	<b>language:</b> VHDL	<b>synthesis:</b> Synplicity
<b>project:</b> ground terminal functions for the Astrolink International Ka-band satellite communications system: 1) ATM cell management. Muxing cell data into transmission blocks via QoS channel-FIFOs; 2) telemetry interface, including bit sampling, encoding/decoding, and packetization, statistics; 3) support functions: uP interface, device serial interfaces. Note that portions of the FPGA used an internal clock rate of 200MHz, which at the time and for this device was stretching the capabilities, requiring locked partitioning and careful pipelining design.				
<b>year:</b> 2003	<b>client:</b> Northrup-Grumman, San Diego	<b>device:</b> XC2V1000	<b>language:</b> VHDL	<b>synthesis:</b> Synplicity
<b>project:</b> software-configurable radio for military aircraft. I developed a control simulator in an FPGA for digital configuration of the radio unit.				
<b>year:</b> 2005	<b>client:</b> Sonoray, San Diego, CA	<b>device:</b> XC2S200	<b>language:</b> verilog	<b>synthesis:</b> vendor sw
<b>project:</b> dental imaging system. I developed the camera image processor, consisting of controlling and collecting the frame shots from the image chip, and then buffering and formatting the frames for delivery to the host software.				
<b>year:</b> 2005,06	<b>client:</b> Nuera, San Diego	<b>device:</b> XC2V1000	<b>language:</b> verilog	<b>synthesis:</b> vendor sw
<b>project:</b> packetized-voice switch. I took over the final development of the central packet routing switch FPGA. Included Gb Ethernet and PCI interfaces.				
<b>year:</b> 2006-09	<b>client:</b> Acorn Technologies (thru Serrano Systems)	<b>devices:</b> XC4VVSX55, V5LX330	<b>language:</b> verilog	<b>synthesis:</b> Synplicity
<b>project:</b> WiMAX pre-IFFT OFDM adaptive filters (two generations). Development consisted of translating MatLab code into FPGA structures. Included extensive DSP processing, implementing proprietary and patented complex adaptive filtering methods.				
<b>year:</b> 2007,08	<b>client:</b> Enerdyne (thru Serrano Systems)	<b>device:</b> XC3S4000	<b>language:</b> verilog	<b>synthesis:</b> Synplicity
<b>project:</b> surveillance drone air/ground link. Interfacing with an on-board drone camera to buffer, packetize, and ground-link				

video. Processing included frame format conversions.				
<b>year:</b> 2008,09	<b>client:</b> ViaSat (thru Serrano Systems)	<b>device:</b> XC4VLX160,XC5VLX30	<b>language:</b> VHDL	<b>synthesis:</b> Synplicity
<b>project:</b> programmable waveform generation for a military aircraft friend/foe identification system. Directed by real-time software, the FPGA generated multiple channels of precise query/response waveforms as part of a simulation environment for testing aircraft transponders. Design included external DDR2 memory interface.				
<b>year:</b> 2010	<b>client:</b> CarrierComm (thru Serrano Systems)	<b>device:</b> XC6SLX45T	<b>language:</b> VHDL	<b>synthesis:</b> vendor sw
<b>project:</b> multi-user framer for a wideband wireless system IDU. Expanded the internal bandwidth and replaced the transport-side radio interface with Gb Ethernet using a newer-generation FPGA device. Gb Ethernet interfaces used Xilinx GTP high-speed SERDES blocks.				
<b>year:</b> 2011	<b>client:</b> Cymer	<b>device:</b> XC6VLX240T	<b>language:</b> VHDL	<b>synthesis:</b> vendor sw
<b>project:</b> develop and characterize a PCIe interface to replace existing proprietary high-speed serial. Used a Xilinx PCIe IP core implemented on a PCIe Xilinx development board communicating with a CompactPCI chassis at x8 Gen2 rate over cable.				
<b>year:</b> 2011	<b>client:</b> Gatan (thru Octera Solutions)	<b>device:</b> Altera EP4SGX110DF29C2X	<b>language:</b> verilog	<b>synthesis:</b> vendor sw
<b>project:</b> multi-channel electron microscope image processing -- background removal, matrix reorganization, and event accumulation. External DDR3 memory for buffering.				

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### Board Development

Prior to 2005 my contract development work also included a variety of board designs, mostly for telecommunications equipment manufacturers, such as Telabs (OC3-based echo-cancelling), Timeplex (ATM AAL1 & AAL5, IMA, T1/E1, DS3/E3, and cell-bearing OC3), Netrix (ATM-bearing DS3/E3 interface w/ traffic shaping and VPI/VCI translation), Licom (STS-1 interface for an add/drop circuit multiplexer), Nuera (OC3 interface), Copper Mountain (PCI/PCI-X platform for data transport of non-fabric-switched traffic), and Cymer (a complete distributed control sub-system for their laser, including analog sensor and control interfaces via a CAN bus).

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### Regular Employment

Prior to 1995 I held a number of positions as a full-time employee, including developing flight simulation with General Electric, SONAR development with Krupp-Atlas in Germany and Singer-Link in MD, TDM and packet switching with GTE, Sprint International, and Netrix (all in VA), Telephony transmission/switching with Licom (VA), and LAN storage with Symmetrical Technologies. From 1986 until the 1995 transition to independent development, I held management positions.

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EDUCATION: BSEE awarded in 1977 by Pennsylvania Sate University. Graduated with high honors.